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Combinational Standard Cell Design using RHBD Technique

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Abstract

In modern digital integrated circuit (IC)design, reliability and performance are critical factors, especially for systems that operate in harsh environments. Combinational logic circuits, integral to many digital systems, are vulnerable to reliability issues, such as radiation-induced failures, which can result in malfunctioning of the device. To address the se concerns,the Radiation-Hardened-by-Design(RHBD)technique has attracted considerable intrest for improving the radiation tolerance of circuits without requiring additional shielding or expensive processes. This paper presents an innovative approach to combinational standard cell design by incorporating RHBD techniques. The proposed method involves utilizing fault-tolerant design principles such as error correction, redundancy, and optimization of logicg at estomitigate the effect so fradiation.The study discusses the selection of appropriate standard cells, the adaptation of combinational logic circuits, and the evaluation of their radiation tolerance. Simulation results demonstrate that the proposed RHBD combinational cells achieve enhanced fault immunity while maintaining area and power efficiency

Keywords: RHBD (Radiation-Hardened by Design),Combinational Logic,Standard Cell,Digital Design,VLSI (Very Large Scale Integration)

I. INTRODUCTION

In the ever-evolving landscape of integrated circuit (IC) design, ensuring the robustness and reliability of digital systems is paramount. This is particularly true for circuits used in space applications, military systems, and high-altitude or radiation-prone environments, where electronic devices are vulnerable to ionizing radiation.Combinational the foundation of many digital systems, face significant challenges in such environments, as they can experience functional failures due to radiation- induced faults.These faults,such as single-event upsets

(SEUs),can lead to in correct logic outputs,potentially compromising the entire system's performance.

Traditional methods of protecting against radiation-related issues, such as physical shielding or the use of expensive fabrication processes, can be inefficient or cost- prohibitive. Consequently intrest in radiation hardened by design technique has been increasing growing interest in Radiation-Hardened-by-Design (RHBD) techniques, which aim to increase the silience of circuits against radiation- induced faults without altering the fabrication process. The RHBD approach focuses on integrating fault-tolerant design principles directly into the standard cell design, allowing for enhanced reliability while maintaining efficiency in terms of area, power consumption and performance. Combinational standard cells are integral components in digital IC design,and ensuring their robustness through RHBD techniques is essential for creating reliable and fault-tolerant systems. In this work,we explore the application of RHBD methods to the design of combinational standard cells.

II. OBJECTIVES

1. ***Radiation Resilience***: The objective of RHBD in combinational standard cell design is to create circuits that are resistant to radiation-induced errors (e.g., SEUs, SETs), ensuring reliable operation in radiation-prone environments like space and military applications.

2. **Performance and Area Efficiency**: RHBD techniques aim to maintain the performance, speed,and area efficiency of the standard cells while enhancing their radiation tolerance, allowing for fault recovery without significant impact on design constraints.

3. **Improved Reliability in Harsh Environments**: For systems deployed in space, high-altitude environments, or military applications,where radiation exposure is significant, RHBD ensures that the circuits continue to function as expected without failure or degradation due to radiation-induced issues.

4. **PerformanceandAreaOptimization**:RHBDfocuses on creating radiation-hardened circuits that maintain the critical design constraints of performance(speed,timing) and area (size of the cells), while also improving their immunity to radiation effects. This involves using design techniques that do not excessively impact the circuit’s performance or increase the are a too much,which is crucial in high-performance applications.

5. **Design Techniques Integration**: The RHBD approach involves integrating various design techniques like redundancy (e.g., triple modular redundancy, TMR), layout modifications(e.g.,shielding),and fault-tolerant architectures into standard cell libraries. These method sensure that the design can recover from transient faults, either through error detection and correction or by preventing the faults from affecting the circuit's operation

III. PROBLEM STATEMENT

Modern electronic systems operating in harsh radiation environments, such as space, high-altitude aviation, and nuclear facilities ,face significant reliability challenges due to radiation-induced effects.These effects, including Single Event Upsets (SEUs) and Single Event Transients (SETs), can cause temporary or permanent malfunctions in digital circuits. Combinational logic, a fundamental building block of these systems, is particularly susceptible to SETs ,which can propagate through the circuit and lead to erroneous

IV. PROPOSED FRAME WORK

A. SOFTWARETOOLSUSED

1. Verilog or VHDL for designing and verifying the circuit
2. Cadence genus tool

SYSTEMARCHITECTURE :

Triple Modular Redundancy (TMR) is designed to increase the reliability and fault tolerance of digital systems, particularly in environments where hardware faults or radiation-induced errors are a concern. The basic idea is to use redundancy to mitigate the effect of errors by replicating key components and introducing voting mechanisms.

1. The typical architecture of TMR:

Triple Replication: **Three Identical Modules**: The system consists of three identical processing modules (or components) that perform the same computation or operation. These modules receive the same inputs.

2. *VoterCircuit:*

Majority Voting: A voter circuit is used to compare the outputs of the three modules and select the majority output. This ensures that if one of the modules produces an erroneous output due to a fault, the correct result is still obtained by considering the majority output of the other two modules.

3. *ErrorDetection andCorrection:*

FaultMasking*: TMRhelpsinmaskingfaultsbyallowing the majority vote to correct a single fault in one module, effectively preventing that fault from propagating to theoutput*

B. **FaultTolerance**:If one module fails(e.g.,due to a radiation-induced error or a hardware failure), the remaining two modules continue to provide correct results through the voting mechanism, ensuring system reliability.

System Architecture Flow:
Input→Module 1→Module 2→Module 3→Voting Circuit → Output

C.IMPLEMENTATION

1.Redundancy Integration via TMR:

Standard Cell Replication: For each logic gate (such as AND, OR, NAND, etc.) in the combinational circuit ,replicate the standard cell three times to create three identical modules (modules 1, 2, and 3). These replicated cells will perform the same logic operation but are designed to be radiation-hardened.

Radiation-Hardened Design: Each of the three standard cells will be designed using RHBD techniques, such as using layout modifications ,shielding ,or fault-tolerant structures, to mitigate radiation-induced errors.

2.MajorityVotingCircuit:

Voting Logic: A**voter circuit**is designed to compare the outputs of the three replicated gates (AND1, AND2, AND3) and select the majority output. If one gate produces an erroneous output, the voter circuit will still output the correct result based on the majority of the gates.

Error Masking: The voter ensures an isolated fault witjin one of the fault in modules (due to radiation or other factors) will not affect the overall output, as long as two of the three modules give the same output.

3.CircuitImplementationSteps:

Design the Combinational Logic: Start by designing the combinational logic circuit you need (e.g., a full adder, multiplier, or logic gate network).

Apply TMR to Each Standard Cell :For every logic gate or combinational cell in the design, replicate it three times (e.g.,for an ANDgate,create three identical ANDgates).

- **Radiation-Hardened Standard Cells**: Apply RHBD techniques to the individual cells. This could involve using larger transistors for greater noise margin, layout adjustments, or using fault- tolerant techniques such as added redundancy, shielding, or differential signaling.
- **Add Majority Voter**: Design and implement a majority voter for each logic block (e.g., a 2-input AND gate) that will select the correct output from the three replicated gates.
- **Connect Voter to Outputs**:Connect the results of the voter circuits to form the end result of the combinational logic.

IV. RESULT

1. Waveform

- The core of TMR is the triplication of the logic. So, for each input signal, you'll effectively see three instances of it, one for each of the redundant logic blocks.
- Each of the three identical logic blocks will produce its own output. The timing diagram will show these three outputs, which should ideally be identical.

- The outputs of the three logic blocks are fed into a majority voter circuit. This circuit determines the final output of the TMR system based on the principle of majority rule.

VI.CONCLUSION

As the demand for reliable digital systems grows,especially in high-radiation environments, the importance of RHBD techniques in combinational standard cell design cannot be overstated. These techniques offer an effective way to enhance the resilience of digital circuits against radiation-induced faults without relying on expensive process modifications or shielding solutions. Through methods like redundancy, error correction, and logic restructuring, RHBD ensures that digital systems can operate safely and effectively in challenging environments, providing critical functionality in aerospace, military, and space exploration applications .By focusing on the desig no fradiation- hardened combinational standard cells, this approach ensures that the fundamental building blocks of digital systems are both high-performance and robust,ready to meet the growing demands of next-generation applications.

VII.REFERNCES

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